WHAT IS CLAIMED IS:

1. An asynchronous circuit for processing units of data having a program order associated therewith, the circuit comprising an N-way-issue resource comprising N parallel pipelines, each pipeline being operable to transmit a subset of the units of data in a first-in-first-out manner, wherein the asynchronous circuit is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained.

2. The circuit of claim 1 wherein the circuit comprises a processor and wherein the N-way-issue resource comprises an instruction pipeline.

3. The circuit of claim 1 wherein N comprises an integer greater than 1.

4. The circuit of claim 1 further comprising an M-way-issue resource, and interface circuitry operable to facilitate communication between the N-way-issue resource and the M-way-issue resource.

5. The circuit of claim 4 wherein M is fewer than N.

6. The circuit of claim 5 wherein M is 1 and N is 2.

7. The circuit of claim 4 wherein M is greater than N.

8. The circuit of claim 7 wherein M is 4 and N is 2.

9. The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the N-way-issue resource to the M-way-issue resource.

10. The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the M-way-issue resource to the N-way-issue resource.

11. The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of first selected ones of the data units from the N-way-issue resource to the M-way-issue resource, and second selected ones of the data units from the M-way-issue resource to the N-way-issue resource.

12. The circuit of claim 11 wherein there is a one-to-one correspondence between the first and second selected data units.

13. The circuit of claim 11 wherein there is not a one-to-one correspondence between the first and second selected data units.

14. The circuit of claim 4 wherein the circuit comprises a processor and wherein each of the N-way-issue resource and the M-way-issue resource comprises one of an instruction dispatcher, a register file, an instruction cache, a branch predictor, an instruction fetch circuit, a writeback circuit, an instruction decoding circuit, an execution pipeline, and branch circuitry.

15. The circuit of claim 4 wherein the interface circuitry is operable to identify selected ones of the data units in the higher order one of the resources for transmission to the lower order one of the resources.

16. The circuit of claim 4 wherein the interface circuitry is operable to transmit selected ones of the data units generated by the lower order issue one of the resources to the higher order issue one of the resources in such a way as to facilitate preservation of the program order.

17. The circuit of claim 1 wherein each pipeline is operable to transmit the units of data in accordance with an asynchronous handshake protocol.

18. The circuit of claim 17 wherein the asynchronous handshake protocol between a sender and a receiver in each of the pipelines comprises:

the sender sets a data signal valid when an enable signal from the receiver goes high;

the receiver lowers the enable signal upon receiving the valid data signal;

the sender sets the data signal neutral upon receiving the low enable signal; and

the receiver raises the enable signal upon receiving the neutral data signal.

19. The circuit of claim 18 wherein the handshake protocol is delay-insensitive.

20. The asynchronous circuit of claim 1 wherein each pipeline comprises a plurality of stages, corresponding stages in each pipeline being interconnected in a state loop operable to communicate state information among the pipeline stages.

21. The circuit of claim 1 wherein the circuit comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

22. At least one computer-readable medium having data structures stored therein representative of the circuit of claim 1.

23. The at least one computer-readable medium of claim 22 wherein the data structures comprise a simulatable representation of the circuit.

24. The at least one computer-readable medium of claim 23 wherein the simulatable representation comprises a netlist.

25. The at least one computer-readable medium of claim 22 wherein the data structures comprise a code description of the circuit.

26. The at least one computer-readable medium of claim 25 wherein the code description corresponds to a hardware description language.

27. A set of semiconductor processing masks representative of at least a portion of the circuit of claim 1.

28. A heterogeneous system for processing units of data having a program order associated therewith, the system comprising an N-way issue resource and at least one multiple-issue resource having an order different from N, the system further comprising interface circuitry operable to facilitate communication between the N-way-issue resource

and the at least one multiple-issue resource and to preserve the program order in all of the resources.

29. The system of claim 28 wherein the at least one multiple-issue resource comprises a plurality of multiple-issue resources having different orders.

30. The system of claim 28 wherein the interface circuitry comprises a dispatch circuit operable to route the data units received from the N-way issue resource on a first number of input channels to designated ones of a second number of output channels associated with the at least one multiple-issue resource in a deterministic manner thereby preserving a partial ordering for each output channel defined by the program order.

31. The system of claim 28 wherein the N-way issue resource comprises first and second pipelines, and the interface circuitry comprises a dual filter comprising a dual-issue input datapath corresponding to the first and second pipelines, a single-issue output datapath, and a control channel, the at least one optional assign being operable to selectively transmit data tokens on the input datapath to the output datapath according to control information on the control channel.

32. The system of claim 28 wherein the interface circuitry comprises remapping circuitry operable to route the data units received from the at least one multiple-issue resource on a first number of input channels to designated ones of a second number of output channels associated with the N-way issue resource in a manner which preserves the program order.

33. The system of claim 32 wherein the remapping circuitry comprises a crossbar circuit which is controlled by routing information generated when the data units are transmitted from the N-way issue resource to the at least one multiple-issue resource.

34. The system of claim 28 wherein the at least one multiple-issue resource comprises an M-way issue resource where M is an integer multiple of N, and wherein the interface circuitry comprises a plurality of split circuits which operate alternately to transmit the data units from the N-way issue resource to the M-way issue resource, and a plurality of merge circuits which operate alternately to transmit the data units from the M-way issue resource to the N-way issue resource.

35. The system of claim 28 wherein the at least one multiple-issue resource comprises an M-way issue resource where M is less than N, and wherein the interface circuitry comprises at least one optional assign circuit which is operable to receive the data units from both of the N-way issue resource and M-way issue resource and to selectively transmit the received data units back into the N-way issue resource, thereby mitigating effects of a difference in throughput between the N-way issue resource and the M-way issue resource.

36. The system of claim 35 wherein the interface circuitry further comprises a crossbar circuit by which the data units are transmitted from the M-way issue resource to the at least one optional assign circuit.

37. The system of claim 35 wherein the at least one optional assign comprises first and second input datapaths, an output datapath, and a control input, the at least one

optional assign being operable to transmit a first data token on the first input datapath to the output datapath when the control input is in a first state, the at least one optional assign further being operable to discard the first data token and to transmit a second data token on the second input datapath to the output datapath when the control input is in a second state.

38. The system of claim 37 wherein the at least one optional assign further being operable to discard the second data token and to transmit the first data token to the output datapath when the control input is in a third state.

39. The system of claim 28 wherein the interface circuitry comprises a dual repeat circuit comprising a single-issue data input channel, a dual-issue data output channel, and a control channel, the dual repeat circuit being operable in response to control information on the control channel to transmit a first data token on the input channel to the output channel and to maintain the first data token on the input channel for future use, the dual repeat circuit also being operable in response to the control information to transmit a second data token on the input channel to the output channel and to discard the second data token so that the input channel can receive subsequent data token.

40. The system of claim 28 wherein the N-way issue resource has N pipelines associated therewith, and wherein the at least one multiple-issue resource has P pipelines associated therewith, and wherein N may be any of fewer than P, equal to P, or greater than P.

41. The system of claim 28 wherein there is a one-to-one correspondence between the data units in the N-way issue resource and the data units in the at least one multiple-issue resource.

42. The system of claim 28 wherein, at any given time, more of the data units are in the N-way issue resource than the at least one multiple-issue resource.

43. The system of claim 28 wherein the system comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

44. At least one computer-readable medium having data structures stored therein representative of the system of claim 28.

45. The at least one computer-readable medium of claim 44 wherein the data structures comprise a simulatable representation of the system.

46. The at least one computer-readable medium of claim 45 wherein the simulatable representation comprises a netlist.

47. The at least one computer-readable medium of claim 44 wherein the data structures comprise a code description of the system.

48. The at least one computer-readable medium of claim 47 wherein the code description corresponds to a hardware description language.

49. A set of semiconductor processing masks representative of at least a portion of the system of claim 28.